ABSTRACT OF THE DISCLOSURE

An enhanced non-volatile semiconductor memory has a source region and a drain region provided in a semiconductor substrate, an electric charge accumulating portion provided on a channel region between the source and drain regions and a control gate provided on said channel region and at least said source region is provided by introducing an impurity in self-alignment with a side wall provided on a side surface of said control gate, characterized in that an overlap of said drain region with said electric charge accumulating portion is set larger than an overlap of said source region with said electric charge accumulating portion, and an impurity dose quantity of said source region is larger than an impurity dose quantity of said drain region. The drain region may be formed by self alignment manner using a first side wall and the source region may be formed by self alignment manner using a second side wall formed on the first side wall.